Dedicated Optoelectronic Stochastic Parallel Processor (OSPP) for real-time image processing: motion detection demonstration and design of a hybrid CMOS/SEED based prototype.

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Abstract

We report experimental results and performance analysis of a dedicated optoelectronic processor implementing stochastic optimization-based image processing tasks in real time. We first show experimental results using a proof of principle prototype demonstrator based on standard Si-CMOS technology and liquid crystal spatial light modulators; we then elaborate on the advantages of using a hybrid CMOS/SEED Smart Pixel Array to monolithically integrate photodetectors and modulators on the same chip, providing compact, high bandwidth intra-chip optoelectronic interconnects. We have modeled the operation of the monolithic processor, clearly showing system performance improvement.

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1. Introduction

Many early and middle vision tasks such as restoration, image segmentation, halftoning or even motion detection can be formulated as optimization problems consisting in finding the ground states of an energy (or cost) function[1]. Stochastic optimization by simulated annealing[2] yield some of the best results because they are not generally constrained to quadratic or even convex cost functions. However, when implemented on conventional sequential workstations, the computational loads are too extensive for practical purposes, so that most of the proposed artificial vision systems rely - one way or another - on *deterministic* optimization algorithms which are at least one or two hundred times faster than stochastic algorithms, but often lead to results further away from optimality.

One can point out two different sources for such a prohibitive computational load. One obvious source is sequential processing of pixels in a two-dimensional image; one way of alleviating this burden might be to process pixels in parallel, using dedicated hardware based on *optical scale parallelism* - by this expression we refer to parallel image processors consisting of one processing element (PE) per pixel. This is possible provided some rules are observed: briefly stated, two pixels that interact on each other should not evolve at the same time; this has led us to the concept of *semi-shift-invariance* and *coloring* in optoelectronic parallel processors[3] (see Fig.1). In the case of *low* level image processing tasks, the state of each PE of the array evolve as a function of a *short*-range shift-invariant interconnection pattern: therefore, stochastic (as well as deterministic) algorithms can advantageously be implemented on single-instruction multiple-data (SIMD) machines with a *high* degree of parallelism. In this context, optical convolution represents an interesting alternative to intra-chip electronic shift-invariant interconnects, because they avoid electronic layout congestion and have the benefits of an easy reconfigurablility of the interconnect topology. The principles of such a mainly digital optical processor architecture, combining electronic nonlinear processing and optical linear

convolution have been studied extensively in the literature under various names including symbolic substitution, mathematical morphology, and cellular automata[4,5,6].

While sequential updating of pixels is a common source of computational load shared with any deterministic algorithm, stochastic optimization algorithms suffer from the additional burden of having to generate good quality, uncorrelated random numbers for every PE in the array; moreover, proper operation of the simulated annealing needs the former operation to be repeated *thousands* of times per image under processing, and even more for complex tasks. In the parallel version of the algorithm, huge amounts of (time *and* space uncorrelated) random numbers need to be generated in order to feed all the PEs of the array at the same time. Electronic (digital) random number generators are not only time and chip-area consuming: they also suffer from the inherent pseudo-random nature of the generated sequence[7]. Based on extensive previous experience[8], we selected differential detection of speckle as a reliable, quick, parallel and easy to control source of random numbers.

We have therefore been studying optoelectronic SIMD machines which are able to minimize low-level image energy functions at video-rate by use of the well-known simulated annealing algorithm. These devices, which we will refer from now on as *optoelectronic stochastic parallel processors* (OSPP) rely on three ingredients: (a) an optical convolution setup in charge of the reconfigurable, shift-invariant interconnection pattern; (b) an optical random number array generator, and (c) an optoelectronic smart pixel array (SPA) to implement the required non-linear operation. So far, only inputs, not outputs, to our SPA have been optical, and convolution has been achieved either electronically (thanks to a hard-wired four-nearest neighbor interconnect) or with the help of an optical convolution setup composed of an interchangeable Dammann grating and a spatial light modulator chip (SLM) interfaced to the SPA trough a - relatively - slow electronic bus: indeed, as we will show, "monolithic"

convolution of the data using a SPA having both optical input and optical output ports would account for an enormous increase of the overall performance of the OSPP system.

The paper is organized as follows: in section §2, we review our present setup, which is to our knowledge, the first complete reconfigurable (non-monolithic) OSPP prototype dedicated to low-level image processing. This proof of principle prototype is based on a silicon CMOS SPA chip. Motion detection at video-rate in a sequence of gray level images is demonstrated. In section §3, the flip-chip bonding technique is considered for building a hybrid Si/AsGa SPA, and figures of merit of this novel OSPP are drawn up as a function of the optoelectronic transceiver characteristics.

2. The present demonstrator

The underlying principles of the Optoelectronic Stochastic Parallel Processor are described extensively elsewhere[9,10]. We report here on our latest experimental illustration, namely the demonstration of video-rate simulated annealing for motion detection in a sequence of noisy gray-level images. The purpose of this demonstrator based on a silicon CMOS SPA is twofold: firstly, it provides a concrete opto-mechanical hardware which should help drawing realistic figures-of-merit while testing novel technologies for the SPA processor; secondly, it constitutes a proof of the good prospect in using stochastic-based algorithms at the core of more complex image processing systems, without compromising the possibility of real-time processing -at least up to video rate.

2.1 Motion detection algorithm

From the point of view adopted in this work, motion detection algorithms and systems provide an output consisting of a binary map ***e***, called the *label field*, indicating motion or absence of it at every pixel of the input (noise-corrupted) gray-level image. There is evidence that motion detection can be achieved using a statistical regularization approach based on spatio-temporal Markov Random Fields (MRF)[11]. Far from being of only academic interest,

motion detection is therefore an interesting demonstration candidate for our video-rate processor.

Specifically, we started from a class of motion detection algorithms first proposed by Bouthemy and Lalande[11]. The original algorithm performs an elementary preprocessing of the sequence in order to prepare two "observed" or "input" data fields. First, a time gradient $\boldsymbol{o}(s,t)$ is obtained by differentiating in time a gray level image, where s is a 2-D pixel coordinate and t is discrete in time. Then, a binary version $\hat{\boldsymbol{o}}(s,t)$ of the time gradient is calculated also, simply using a pre-defined threshold. The energy function to be minimized (as a function of the 2-D label field $\boldsymbol{e}(s,t)$ under estimation) incorporates both "input" fields as well as the previous state of the label field $\boldsymbol{e}(s,t-dt)$.

In our setup, the host computer is in charge of all the preprocessing. While we started from the Bouthemy and Lalande algorithm, we found out that it was necessary to introduce some simplifications to it before parallel optoelectronic implementation could be envisaged. Specifically, the need for two time-gradient input data fields $\boldsymbol{o}(s,t)$ and $\hat{\boldsymbol{o}}(s,t)$ was a problem. However, we concluded from simulations that it is worthwhile to investigate a model where only the binary (thresholded) version $\hat{\boldsymbol{o}}$ of the image gradient is used as input to the algorithm. The whole idea relies on the assumption that the state of motion is likely to change *only* if temporal changes are notable - this is the case for a pixel located on the edge of a moving object. Otherwise, we would prefer the label to retain the value held in the near past. Spatial regularization potentials are also defined in such a way as to favor homogeneous regions of motion. A schematic representation of the underlying principles of the simplified algorithm is shown in Fig.2. It is appropriate here to mention the difference between motion detection and the mere subtraction of successive frames in a time sequence: a non-zero difference between two consecutive images may indicate motion, but it may as well be due to time variable noise or a change in illumination conditions; on the other hand, a null difference may be the result of

subtracting consecutive pixel values at two different locations in the body of a uniformly lit moving object (see Fig.3). The purpose of motion detection is to give a *complete* estimate of all pixels in the scene that are moving at a given time, and follow their motion in terms of compact, but deformable, moving objects.

As expected, estimation of the current label field only involves very local computations: the local energy gradient with respect to the label variable only depends on a short-range neighborhood around the pixel under consideration. Various strategies have been proposed for the order of site visiting (at random, by sequential scanning, or using a "confidence" ordering list to accelerate the relaxation process as in[12]). However, as explained above, parallel updating of sites happens to be the fastest strategy since the neighborhood size reduces to the four/eight nearest neighbors. Also, while many deterministic optimization algorithms require paying a lot of attention to the label field initialization procedure (ultimate quality of the result strongly depends on it[13]), stochastic-based algorithms completely relax such a constraint.

In short, all a PE has to do is:

(a) To calculate the local "force" (i.e. the local energy gradient at a particular site *s* and time *t* with respect to the label variable), which combines one regularization term F_S and a second (conditional) constraint-to-the-data term F_C:

$$\begin{aligned} F(s,t) = \beta_S \sum_{r \in N(s)} \left(2e(r,t)-1\right) \qquad & (= F_S) \\ +\beta_C \left(2e(s,t-1)-1\right)\left(2\hat{o}(s,t)-1\right) \qquad & (= F_C) \end{aligned} \tag{1}$$

In the above expression, *N(s)* represents the neighborhood of pixel *s* and β_S and β_C are empirically determined constants. The term F_S(t) can be seen as a regularization *field*, resulting from a convolution between the current field *e*(t) and a short-range (equally weighted) convolution kernel. The term F_C(s,t) behaves as a conditional constraint to the label field data held in the near past (memory effect), provided that no significant "change" has been detected in the particular site (i.e. the variable $\hat{o}$(s,t) is zero); otherwise it tends to *flip* the label state, as

explained above (Fig.2). Our simulations have shown proper operation of the algorithm provided that the ratio $\lambda=\beta_C/\beta_S$ lies between 0.4 and 1.2.

(b) Update its label ***e***(s,t) according to the *sigmoïd* probability law:

$$\Pr\{e(s,t)=1\} = \frac{1}{1+\exp[-F(s,t)/T]} \qquad (2)$$

This is performed by simply thresholding on the local force F(s,t) by a standard electronic comparator; the nature of such deterministic operation is turned probabilistic thanks to a laser speckle generator which projects a time-varying speckle light over two photodetectors attached to both positive and negative inputs of the comparator (the decision threshold is therefore "randomly shaken"). Characterization of these "stochastic comparators" (or "random number generators") is given in detail in[14].

Thanks to operations (a) and (b), the updating of a particular PE state is thereupon achieved. Updating can be done in parallel on pixels that do not directly interact with each other. Maximal sets of pixels that do not interact are said to belong to the same "color" domain, and colors domains are to be considered sequentially. As a result, the entire field ***e***(t) is eventually updated. It should be reminded here that two "neighboring" (i.e. interconnected) processor cells never have the same color; therefore, as the size of the neighborhood increases, so does the number of color domains (see Fig.1). The process iterates following the *annealing* schedule by decreasing the speckle laser power which represents the (algorithmic) temperature (T) of the annealing[1,2]. With this simply algorithm, one "serious" simulated annealing operation consists in typically one thousand updating cycles of the whole field ***e***(t).

2.2 Smart pixel array hardware

Because of the general availability and maturity of silicon technology, in an earlier collaborative project with IEF, CNRS/Université de Paris-Sud[15], we developed a CMOS SPA, named SPIE600, consisting of 24x24 identical processor cells for the optoelectronic simulation

of an Ising spin array with two phototransistors per cell serving as optical inputs for the speckle light, used to compute the updating probability of Eq.(2) by differential detection of speckle [16]. Of course, because light emission by silicon is far from being well mastered, there is no optical output. The optical inputs, however, are sufficient for the Ising spin problem. Although indeed, the optical inputs may be used for the neighborhood convolution as explained in the introduction, a provision for electronic bipolar interaction to the four nearest neighbors has been implemented. This work has been published earlier, demonstrating video-real time massively parallel implementation of an Ising spin array[17].

It appeared that the same chip could be used for demonstrating some low level image tasks. For instance, it could be used for noise cleaning on binary images - a problem of only academic interest though - by simply setting all interaction coefficients of the Ising chip to unity, and then *optically inputting the binary image to be processed* (dual-rail encoded as explained in ref.[4]) onto the photodetectors on the chip. This is possible because each PE is provided with two optical inputs. This was actually done as the first full experimental demonstration of an OSPP for image processing (noise cleaning in binary images) at video-rate, exploiting the concept of semi-shift invariance by coloring[18]. In the present work, optical convolution and electronic feedback have been added to the OSPP to broaden the interconnection neighborhood, while the task demonstrated is motion detection. This will be explained in some detail below.

2.3 System architecture

There is a fundamental interest in studying and evaluating the performances of an optically interconnected prototype, and the noise-cleaning OSPP demonstrator lent naturally to this kind of experiment. Indeed, optical inputs to the PEs can be used as channels for communicating *between each other*, provided that theirs outputs are made somehow optically available. As explained in §1, optical convolution is an interesting solution for the interconnection hardware because all contemplated applications of the OSPP (noise cleaning, halftoning, motion

detection…) need a shift-invariant interconnection pattern. Moreover, as the interconnection topology depends on each particular application, an easy way of reconfiguring it is also welcome. Optical convolution also provides extension to larger convolution kernels, neither compromising the electronic complexity of each PE or the density of the array.

With respect to the noise cleaning demonstrator mentioned above, two major improvements were required: (1) two SLMs were added in the system : one for optically generating the constraint-to-the-data (precalculated) binary *field* F_C(t) of Eq.(1), and the other to perform the convolution in an optoelectronic feed-back loop, using a convolution filter (a two level-phase Dammann grating in our experiment), so that regularization term F_S of Eq.(1) would become optically available (see Fig.4). Of course, the optical feed-back was implemented using a bulky optical setup significantly increasing the demonstrator volume. The on-chip electronic interconnects were disabled. (2) All the optical parts of the demonstrator and the associated mechanics had to be designed for easy adjustment, stable operation over a long period of time, and easy transportation e.g. for presentation at seminars and conferences. Figure 5 represents a view of the complete setup. Details of the optomechanic implementation and testing of the non-monolithic macro-optical prototype will be published in an article presently under preparation.

2.4 Experimental results and demonstration.

The demonstration of the modified Bouthemy-Lalande algorithm was successfully completed using the OSPP prototype described above, yielding good quality moving pixel estimates over synthetic noisy gray-level moving sequences (see Fig.3). While video rate was compatible with the components, non optimal operation of the Windows computer interface operating with the driving PC slowed the process to about 5 seconds per full simulated annealing when using the four nearest neighbor interconnecting hologram (the array is then divided into two different "colored" domains, see Fig.1) and to about 24 seconds in the case of an height nearest neighbor interconnecting hologram (leading to four colored domains, see

Fig.1). Because our images are 24x24 pixel large, the level of parallelism is respectively 24x24/2 =238 in the case of the four nearest neighbor interconnected array, and 24x24/4=119 in the case of a wider 8 nearest neighborhood interconnection pattern. For a fixed interconnection pattern, the level of parallelism scales with the number of pixels and is only restricted by the cost of dedicated chip design and fabrication. The SPIE600 chip was designed in 1994; with the presently available technology, it would be possible to design a new version of the chip with many more pixels, perhaps several hundreds on a side, and the processor operation would be exactly as fast.

3. Design of an hybrid CMOS/SEED based OSPP prototype.

If video-rate stochastic processing is to be achieved along with good results in terms of quality of the optimization (that is, at least one thousand updating cycles per annealing), then our optically interconnected SPA has to be provided with an optoelectronic feed-back working at rates higher than 25*1000*N_C loops per second (where N_C represents the number of colors domains in the processor). Actually, our current OSPP demonstrator uses a binary ferroelectric liquid crystal SLM chip (FLC/IC) for feed-back and convolution; even if we neglect the time needed for reading and properly formatting the data flowing trough the electronic loop (controlled by a 100MHz Pentium host computer), the SLM full frame rate is less than 2 kHz - more than 20 times under the minimum required rate in the simplest case of two-color operation of the processor array, so that only hardly 50 updating cycles could in principle be achieved at video-rate - a less than satisfactory situation. As a matter of fact, placing sources and detectors in different chips is an unsatisfactory solution since it leads to an electrical bottleneck when routing a full 2D binary data-field from one chip to another. This is indeed what limits the SLM full frame rate. We thus contemplated the design of a new version of the OSPP, relying on a unique SPA in which all PEs would be electronically isolated from each

other (except for the clock and probably some additional control signals), and would include *in situ* high bandwidth optoelectronic transducers.

3.1 OE-VLSI chip architecture

It is appropriate at this stage to review the operation of an optically interconnected version of the OSPP. Each PE of the SPA would require the following features:

(1) As presently, a pair of photo-detectors to implement the probabilistic updating by differential detection of speckle. These inputs are also used to calculate the local force F_S(s,t), by analogous (intensity) addition of the neighborhood output optical signals. It is interesting to notice that differential encoding allows robust operation under low-contrast input data conditions, which is generally the case when the signal is provided by some kind of modulator-based source;

(2) A comparator (point non-linearity), in charge of the thresholding operation that sets every PE into its new state;

(3) A one bit memory, defining the current state of the PE;

(4) Since this state has to be read by the neighborhood PEs, it has to be directed to a dual-rail optoelectronic output; these can be either sources (LEDs or VCSELs) or modulators such as p-i(MQW)-n diodes.

The basic PE design then corresponds to a differential receiver enhanced with an optoelectronic transmitter device (known in the literature as *differential transceiver* or *two-beam transceiver*)[19]. Recently, there has been significant progress in the development of these for data-communication and information-processing purposes, and many publications account for well-characterized and functional optoelectronic transceivers[19,20]. The efforts in designing our elementary processor are then considerably reduced.

To make the coloring of the SPA easily reconfigurable, we can add an additional feature :

(5) a three bit memory to encode the corresponding PE color (5 colors are enough for a 12 nearest neighborhood interconnected SPA) along with a binary counter, so that only one common clock signal (ticking the binary counter) would be needed to control the sequential updating of colors domains (this signal may be provided optically as well). Also, the whole optical architecture of the OSPP demonstrator can be greatly simplified (saving one SLM and its corresponding optical arm) with a final improvement:

(6) an additional one bit memory for storing the constraint-to-the-data term F_C(s,t) during the whole simulated annealing process. Sequential loading of color numbers as well as the pre-calculated binary constraint-to-the-data *field* F_C(t) can be done in parallel over the rows of the array before the simulated annealing iterations are started. The technique has been tested on the present chip SPIE600: a full loading of the chip registers can be done in less than 3 μs, which would hardly affect the 40ms needed to perform simulated annealing at video-rate. The schematic of a single PE with one dual-rail optical input and one dual-rail optical output is shown in Fig. 6. The optical architecture of the optically interconnected OSPP is shown in Fig.7. A holographic array illuminator (AI) creates an array of reading beams to be projected onto the PE *modulators*. Thanks to a cube beam-splitter and a computer generated hologram (CGH), the resulting reflected signals (from the modulators in the ON state) are convoluted and instantaneously back-projected to the photodiodes of the SPA (a process which we referred to earlier as "monolithic feedback"). Relative weighing of each contribution F_S and F_C to the local force of Eq.(1) is done by adjusting the power of the optical source with respect to a fixed electrical input to the chip (the "constraint term β_C" input line of Fig.6).

3.2 Optoelectronic transducers

In comparing different input-output devices, one has to consider several competing parameters such as power consumption and dissipation, sensitivity, response time and driver layout area. Better optoelectronic transducers do not only lead to improved performances of the

whole system; they also potentially broaden the range of applications for a given optical power (higher sensibility allows wider convolution kernels without additional optical power requirement). Liquid crystal modulator-based smart pixels are limited to response times in the microsecond regime; as far as response time is concerned, there is a gap between these devices and semi-conductor receiver/transmitter-based smart pixels (typically hundreds of MHz). Although performances of the latter may seem to exceed our needs (response times of about one tenth of a μs would just do it) we are obliged to consider semi-conductor devices since liquid-crystal microsecond regimes are unacceptable. Table 1 summarizes other possible technologies, along with the corresponding maximum (estimated) simulated annealing rates, based strictly on response time; the next section will have a much more detailed investigation of one of the technologies. Our selection of the technology was based on data directly available to us on two types of smart pixel arrays:

- AsGa photothyristor array chips, and hybrid CMOS/SEED chips,
- AsGa multiple quantum well self-electro-optic-devices (MQW-SEED)[21] flip-chip bonded to standard Si-CMOS circuits.

Photothyristor pairs. At first sight, an array of AsGa differential photothyristor pairs[22] seems to fulfil all the requirements (i.e., differential detection and one-bit memory thanks to optical bistablility) without the help of any additional electronics[23]. High sensitivities of 2,6 fJ at 720 nm have been reported, and optical cascaded transmission between arrays has been demonstrated at rates as fast as 50 MHz[24]. We were fortunate to be able to test one integrated circuit composed of 32 PnpN photothyristor pairs made available to us by IMEC[25]. The matrix was laid out in a checkerboard fashion, with one separate voltage supply for each interlaced matrix (bipartitioning of the processor is hard-wired, as in SPIE600, therefore automatically ready for two colors operation). Unfortunately, our measurements on this particular device indicated poor overall performances: the average detection threshold turned out close to 1,2 pJ

at 783 nm (far from the fJ regime), and the average total power emitted per site (at 860nm) was about 31nW. Our photothyristor array suffer from three major drawbacks: a) an important mismatch between pairs (four elements were useless in our circuit); b) low sensibility (about 100 times lower) at its own emission wavelength, severely compromising the all optical interconnection issue; and c) important divergence (LED-lambertian source) which leads to cross-talk and insertion loss, and imposes the use of additional imaging optics to concentrate their energy (micro-lens array, for instance). It is possible to switch a photothyristor using the light emitted by its neighbors, but, even considering null optical losses, the feedback loop would be very slow: 31 nW/(100x1,2pJ) = 26 ms with the devices that we tested. Hence, no more than one serious simulated annealing process (composed of one thousand updating cycles) would be possible every 2,6 seconds, which does not meet the requirement for a video-real time OSSP demonstrator. We understand from the latest publications on this device (ref 23) that better performance was achieved from later devices, but unfortunately, to our knowledge, such devices are no more being developed.

Hybrid CMOS-SEED technology. Rather than compete with CMOS technology, hybrid CMOS-SEED technology[26] seeks to complement it in the interconnection domain by providing additional high-density, high-bandwidth optical inputs and outputs to the existing electronic circuitry. Performances of the flip-chip bonded GaAs-MQW modulator/detectors depend strongly on the design of its driving (CMOS) circuit. Operation of a two beam, differential receiver-transmitter circuit at a rate of 620 Mbit/s and a sensitivity of 30 fJ per beam has been reported using transimpedance front-end amplifiers (TIA)[19]. Almost 100% device yield for large arrays (68x68) has also been demonstrated[20]. Operating such devices at normal incidence with collimated light simplifies the imaging system (divergence is only due to diffraction). In short, CMOS-SEED technology currently available offers fairly good performance while

considerably reducing the effort in designing our PE, since well characterized and tested standard transceiver cells are available from many university research groups.

The following section is devoted to establishing a theoretical upper bound for the frequency of operation of an OSPP demonstrator using a CMOS/SEED SPA device. Two different receiver front-end amplifier circuits will be considered: TIA amplifiers and charge-sense amplifiers (or CSA). The methodology used in the present study is strongly inspired by earlier works of one of the authors [27].

3.3 Optical and electronic power budget

The purpose of this section is to derive an upper bound for the operation frequency of the monolithic OSPP demonstrator (i.e. its feed-back rate), depending on the total optical and electrical power available on the system, and the maximum thermal dissipation of the SPA.

Optical power limitations. We will consider quasi-CW mode of operation of the external optical laser source (the "reading" laser), we will also assume a maximum power of 1 Watt. The photodetectors used to convert the optical signal into current or voltage variations are p-i(MQW)-n photodiodes, having at least (an average) responsivity of S≈0,5A/W. The voltage output from the electronic circuitry modulates the device into high R_{ON} (typically 70%) or low $R_{OFF}=R_{ON}/C$ reflectivity levels (C is the contrast ratio of the modulator -typically C≈2:1).

In order to estimate the overall system performance (i.e. maximum frequency of operation of the feedback loop), we have to determine the lossiest optical path from the source to the detectors of the SPA. Optical losses have been extrapolated on the realistic basis of our previous prototype demonstrator described in section 2. Maximal losses occur on the route going from the laser source of total power P_{tot} to a particular modulator - e.g. the "plus" modulator of PE(j):

$$p_m(j) = \eta_{S-PE} P_{tot}\,, \tag{3}$$

and then, from there to the "plus" photodiode of PE(*i*) (a neighboring PE, see Fig.8) leading, if PE(*j*) was in the ON state, to the optical power:

$$p_d^{ON}(i) = \eta_{PE-PE}\, R_{ON}\, p_m , \tag{4}$$

and if PE(*j*) was in the OFF state :

$$p_d^{OFF}(i) = \frac{p_d^{ON}(i)}{C} = \eta_{PE-PE}\, \frac{R_{ON}}{C}\, p_m . \tag{5}$$

The efficiency of the path from the laser source to a particular PE modulator, $\eta_{S\text{-}PE}$, depends on the efficiency and the fanning-out of the array illuminator. We safely assume an efficiency of 40% for the AI in the case of a Dammann grating, (and perhaps up to 70% using Talbot holograms[28]). We have then $\eta_{S\text{-}PE}$ = 40% / (2xN_{PE}), where N_{PE} is the number of PEs in the SPA, and the factor 2 accounts for the two photodiodes per PE. The fan-out efficiency of the interconnecting hologram, $\eta_{PE\text{-}PE}$, depends on neighborhood under consideration. The two-level phase Dammann grating used in our previous demonstrator has shown 16%, 9% and 7% efficiency respectively in the case of a 4, 8 and 12 nearest neighbors interconnection pattern (leading to a total efficiency of 64%, 72% and 84% respectively). The *minimum* optical power that has to be detected by PE (*i*) (e.g. when a unique neighboring PE flips its state) is given by:

$$\begin{aligned} p_{\min} &= 2\left(p_d^{ON} - p_d^{OFF}\right) = 2\, p_d^{ON}\left(1-\frac{1}{C}\right) \\ &= 2\,\eta_{S-PE}\,\eta_{PE-PE}\, R_{ON}\left(1-\frac{1}{C}\right) P_{tot} \end{aligned} \tag{6}$$

For a total optical power P_{tot}=1 Watt and a state of the art 32x16 pixel large array, p_{min} ranges from 52 μW in the case of a simple mesh-interconnected array, 29μW in the case of a 8 nearest neighbor interconnection, and 24 μW in the case of a wider 12 nearest neighbor interconnect topology.

The optoelectronic conversion time T_{IN} (from optical signal to logic level voltage) depends on the front-end amplifier in use. We have considered here a diode clamped receiver (DCR)

front end amplifier. In this case, the energy carried by the optical signal of power p_{min} has to be sufficient to produce a small voltage swing ΔV_{in} about the threshold voltage of the input transistor of the diode clamped receiver (see Fig.9). We consider here a clamped-diode single-stage voltage amplifier with zero output conductance as in[29]. In order to be detected, the pulse duration τ_o times its power p_{min} must satisfy the following condition:

$$p_{\min}\,\tau_o \geq \Delta E_{\min} = \frac{1}{S} C_{in}\,\Delta V_{in}\,, \tag{7}$$

where C_{in} is the total output capacitance formed by the detectors, the bonding pad and the input transistor gate ($C_{in}\approx 300\ fF$). If the Eq.(7) is satisfied, then the sum of the conversion and amplification times is given by[30]:

$$T_{IN} = \frac{3}{4}\frac{C_{in}\,\Delta V_{in}}{S\,p_{\min}} + 2\,C_{out}\,\frac{\Delta V_{\log}}{g_m\,\Delta V_{in}}\ , \tag{8}$$

where C_{out} ($\approx 120fF$) is the output capacitance of the amplification stage, and g_m is its (constant) transconductance ($\approx 10^{-3}$ S); $\Delta V_{\log}$ is the typical logic-level voltage swing ($\approx$1 V).

In the quasi-CW mode of operation (the duration of the reading pulse is $\tau_o = T_{conv}$), and during the updating cycle of one PE, the output modulators are driven to a high or low reflectivity state *prior* to the illumination by the reading beams (see chronogram in Fig.10), so that the "output" switching time is simply given by:

$$T_{OUT} = 2\frac{C_{ex}\,V_o}{\Delta I_{trans}}, \tag{9}$$

where V_o is the voltage applied to the modulator (8V), C_{ex} is the output capacitance of the smart pixel, and ΔI_{trans} is the current flowing to the output capacitance. Typically, $T_{OUT} \approx$1ps.

The total on-chip processing time T_{PE} is given by:

$$T_{PE} = T_{IN} + T_{elec} + T_{OUT}\,, \tag{10}$$

where T_{elec} is the electronic processing time determined by SPICE simulation (typically tens of nanoseconds for CMOS technology). The clock period must exceed the total "system" processing time:

$$T_{PE} + T_{flight} \le T_{clock} = \frac{1}{F_{clock}}, \tag{11}$$

where T_{flight} is the time of flight of the optical signals (in the order of one nanosecond in our architecture). The updating rate of each color domain (i.e. the feedback rate) is simply $F_C = F_{clock}/N_C$. An upper bound for the frequency of operation is then given by the following equation:

$$P_{opt} = \frac{3}{8} \frac{\Delta E_{\min}}{\eta_{S-PE}\, \eta_{PE-PE}\, R_{ON} \left(1 - \frac{1}{C}\right)} \left[\frac{1}{F_C} - \frac{N_C}{F_{MAX}} \right]^{-1} \le P_{tot} \ , \tag{12}$$

where

$$F_{MAX} = \frac{1}{T'_{amp} + T_{elec} + T_{OUT} + T_{vol}} \approx 83 MHz \tag{13}$$

is an upper bound for the clock frequency, independent of the total optical power available on the system and depending exclusively on the electronic circuit and the optical architecture characteristics.

Electrical power budget and thermal limitations. We calculated the electrical and thermal budget, and we found that for a reasonable heat removal capability of the array Q of the order of 10 W/cm², and a usual electrical power supply of 5 W, the 16x32 SPA under study is only *optical power limited*.

3.4 System performance

Figure 11 shows the laser power consumption for a 32x16 array-based monolithic OSPP, as a function of the frequency (clock) operation, in the case of three different interconnection patterns. Table 2 summarizes the overall performances of the proposed compact prototype, in

terms of simulated annealing operations per second. Although the estimation of 150.10^3 annealing cycles per second (Tab.1) was too optimistic, the performance of the new OSPP remains at least three order of magnitude above the video-rate regime. It is important to say here that with our current speckle generator configuration (using a rotating diffuser), up to 100.000 spatio-temporal uncorrelated speckle fields can be generated per second, which is large enough for a video-rate "serious" simulated annealing, but is too short if thousand simulated annealings are required per second. However, it has been shown that using an alternative speckle generator hardware (based on cavitation noise), it is possible to overcome this limitation[14].

To our knowledge, dedicated electronic video-processing hardware does not perform better (in terms of processing rate) at statistical regularization-based (Markov Random Field based) motion-detection tasks. For the sake of comparison, let us mention a *general purpose* vision system (powerful and versatile, yet rather expensive and cumbersome), the TRANSVISION system (1991)[31], able to process up to 2 images/second when configured for MRF-based motion detection, and a *dedicated* (thus cheaper) DSP-based hardware, the PCMARKOV[32] PC compatible card designed exclusively for motion-detection (1996), capable of a maximum processing rate of 3 images/second. These system are able to process standard resolution (256x256 pixel large) images, instead of hyper-low resolution (24x24 or 32x16) images; but as explained before this is just a different issue, concerning the technologically-achievable SPA density. The OSPP is a parallel processor; hence, there is *no* trade-off between SPA density and frequency of operation - the latter depending solely on the PE optical input/output bandwidth.

Figure 12 shows the expected aggregate optical bandwidth (or aggregate capacity) achieved using a 32x16 hybrid-CMOS/SEED based OSPP prototype (the aggregate optical bandwidth of the system is defined as the average input/output bits per second flowing within the free-space 2-D optical bus during the annealing process). Figure 12 also draws a comparison between our

OSPP prototype and other recent optoelectronic system-demonstrators (photonic switching systems, free-space optical backplanes, etc.) using one or more SPAs. Indeed, aggregate capacity can be seen as a general system performance indicator, resulting - in the case of the OSPP - from the (feedback rate) x (size of the image) product, divided by the number of colored regions of the semi-shift invariant SIMD processor. The feedback rate (or clock frequency F_{clock}) divided by the number of colors N_C corresponds to the *individual optical bandwidth* of the PE input/output differential channel (which strongly depends on the transducer technology). On the other hand, the connectivity of the system refers to the number of optical input/output channels present on the system.

Figure 13 shows improvement on the prototype compactness. The system interconnection density refers to the total optical interconnection length (i.e., the collected length taking every optical path within the system) divided by the total volume of the demonstrator. For an optoelectronic system based on free-space 2-D interconnected arrays, there is a theoretical upper bound for the interconnection density, given by $D=L/V=2\pi/\lambda^2$, where λ is the wavelength of light used within the system[33]. For instance, if we consider the former standard 850nm wavelength for optical communications, the interconnection density is about 8700km/cm^3 - at least seven orders of magnitude above that of present demonstrators. Nevertheless, the goal is that the final size of the whole OSPP"module" be compatible with standard multi-chip electronic boards, which is likely to be a realistic aim considering that the random number rotating diffuser does not need to be more bulky than a conventional heat-removal motorized fan.

4. Conclusion.

We have described the first reconfigurable optoelectronic stochastic parallel processor (OSPP) dedicated to real-time (low-level) image tasks. Design and testing of a non-monolithic free-space interconnected prototype (an SLM is required in addition to the silicon-SPA) have

been completed; we successfully demonstrated application of this system to motion detection in gray-level (synthetic) image sequences. Hardware reconfiguration of the OSPP involves rearrangement of the shift-invariant intra-SPA interconnection topology; this was achieved in our first prototype by simply replacing the optical filter used within the non-monolithic convolution setup. In fact, this (bulky) optomechanical hardware only simulates intra-chip interconnects trough a relatively slow electronic feedback loop, which is responsible for the relatively poor overall system performance. Theoretical modeling shows that the later can be notably improved by the use of a hybrid CMOS/SEED based SPA (capable of both optical input and output of signals), and a "monolithic" convolution setup. Indeed, even for the contemplated "slower" configuration (N_C=5), up to 12800 images can be processed per second, outperforming most dedicated electronic image processing systems - even when these rely on fast deterministic optimization algorithms. We also pointed out that the integration of a complete OSPP module in a conventional electronic board can be considered a realistic goal.

With this first complete OSPP demonstrator we hope to have drawn some of the attention we think this approach deserve in the field of dedicated hardware for video real-time image processing. Theoretical modeling of an hybrid CMOS/SEED based OSPP should also pave the way for the implementation of more compact and powerful prototypes to come. This study represents one of the possible pathways for the introduction of novel optoelectronic devices in dedicated image processing systems; nevertheless, application of the OSPP to neural-network like signal processing systems can be contemplated if non shift-invariant and reconfigurable intra-chip interconnects were made somehow available within the SPA - an issue far beyond the scope of the this paper but that is worth to be investigated[34,35,36].

5. Acknowledgments

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thesis of Alvaro Cassinelli at the Institut d'Optique. Philippe Lalanne and Donald Prévost participated actively in previous stages of this work. The essential role of Eric Belhaire, Francis Devos, Antoine Dupret, Patrick Garda, and Jean-Claude Rodier in designing and testing the SPIE600 chip is gratefully acknowledged. We also wish to thank André Villing for his contribution to the design of the demonstrator electronic driving circuits.

FIGURES

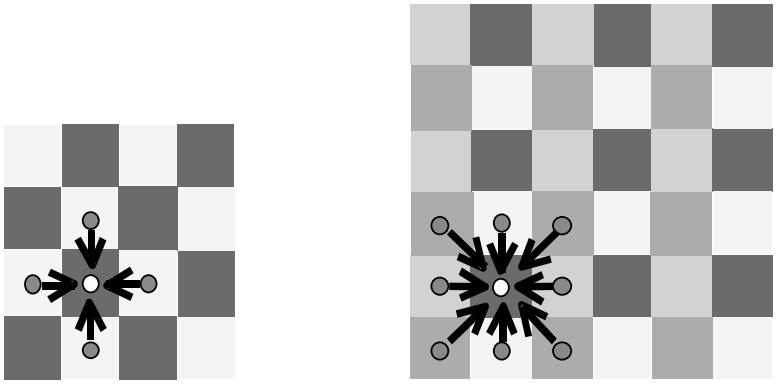


FIGURE 1

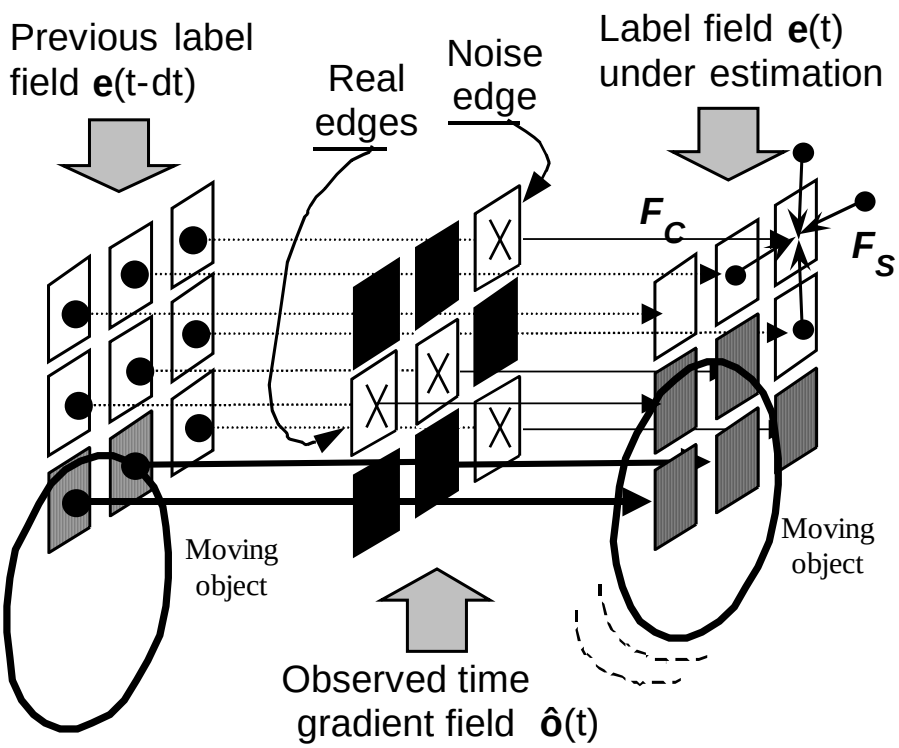
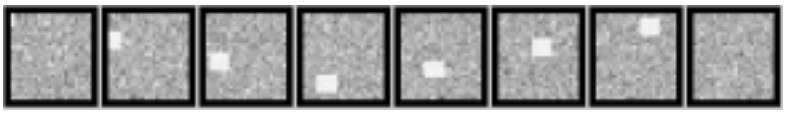
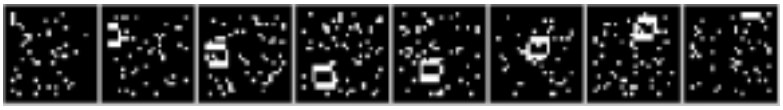

Previous label field **e**(t-dt)
Real edges
Noise edge
Label field **e**(t) under estimation
F_C
F_S
Moving object
Moving object
Observed time gradient field **ô**(t)

FIGURE 2

Synthetic gray level sequence (one frame out of three)



Change detection field (or "observed" binary field **ô**)



Motion-detection mask (binary field **e**)

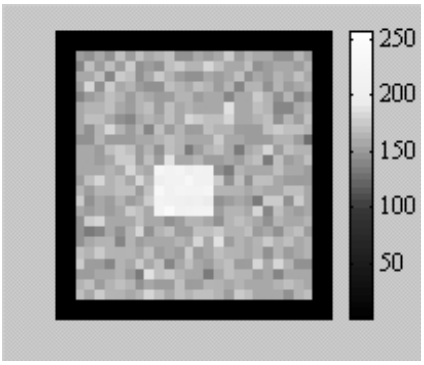


FIGURE 3

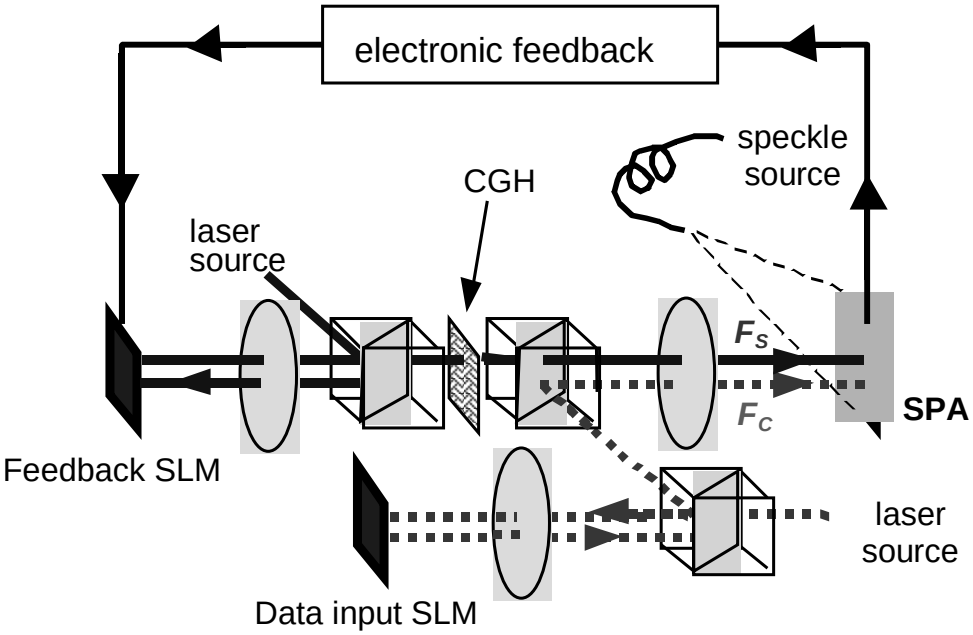

electronic feedback
speckle source
CGH
laser source
F_s
F_c
SPA
Feedback SLM
laser source
Data input SLM

FIGURE 4

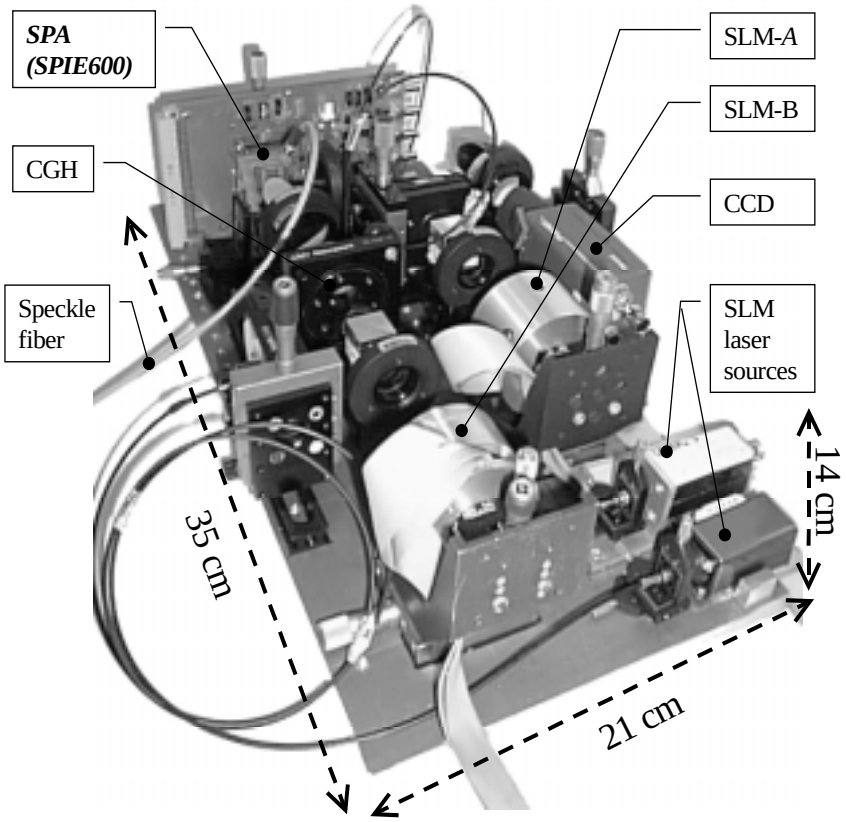

SPA
(SPIE600)
CGH
Speckle
fiber
SLM-A
SLM-B
CCD
SLM
laser
sources
35 cm
14 cm
21 cm

FIGURE 5

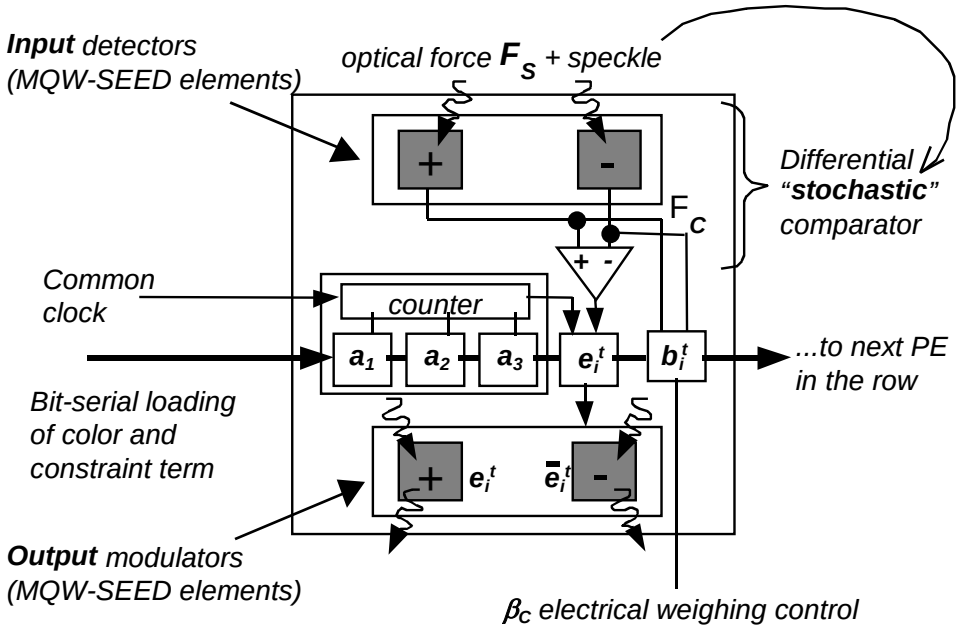

Input detectors
(MQW-SEED elements)
optical force F_S + speckle
+
-
Differential
"stochastic"
comparator
F_C
+ -
Common
clock
counter
a_1
a_2
a_3
e_i^t
b_i^t
...to next PE
in the row
Bit-serial loading
of color and
constraint term
+
e_i^t
$\bar{e}_i^t$
-
Output modulators
(MQW-SEED elements)
β_C electrical weighing control

FIGURE 6

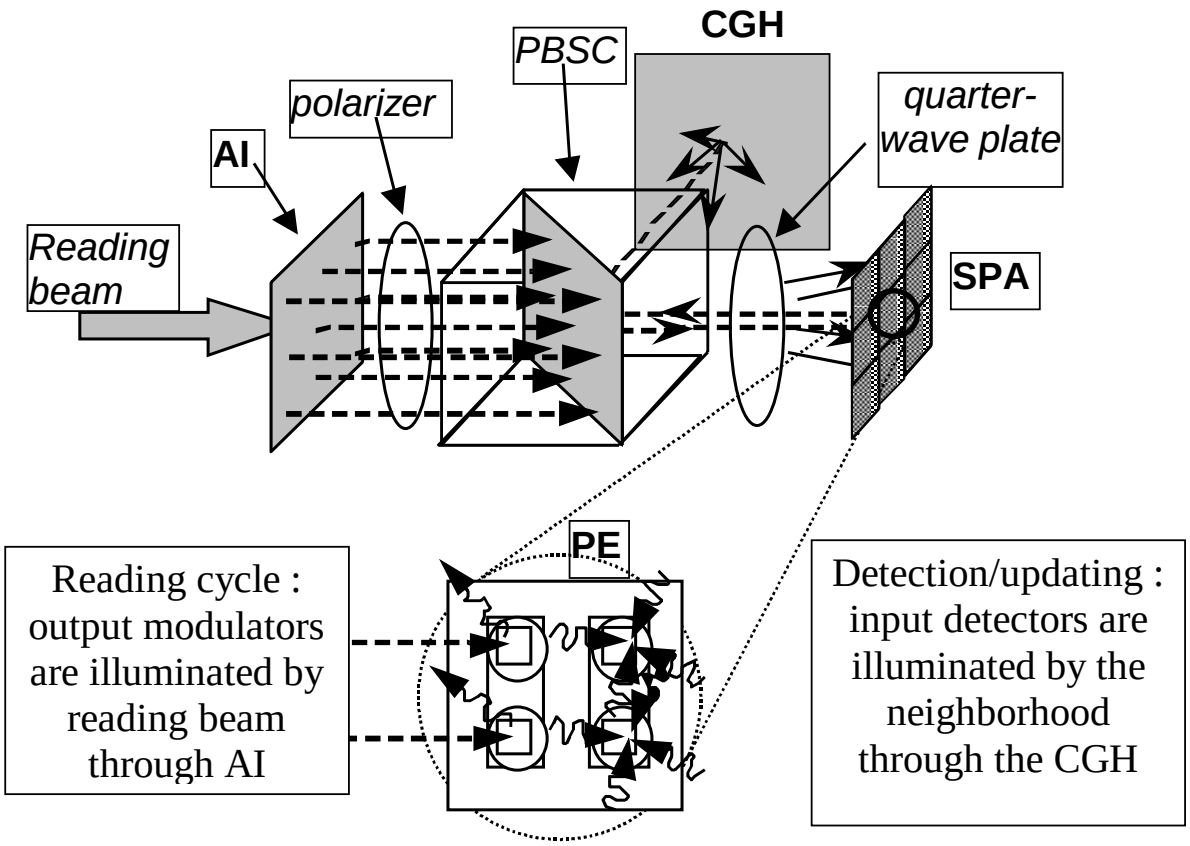

CGH
PBSC
polarizer
AI
quarter-wave plate
Reading beam
SPA
PE
Reading cycle : output modulators are illuminated by reading beam through AI
Detection/updating : input detectors are illuminated by the neighborhood through the CGH

FIGURE 7

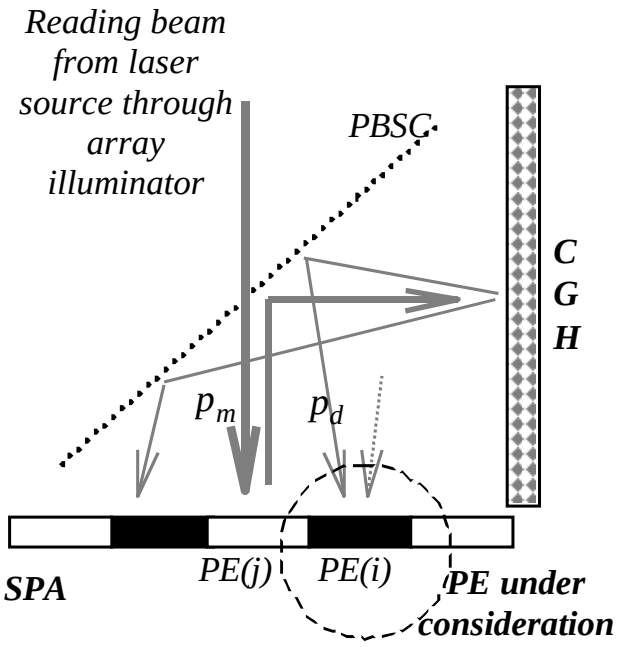

Reading beam from laser source through array illuminator
PBSC
C
G
H
p_m
p_d
SPA
PE(j)
PE(i)
PE under consideration

FIGURE 8

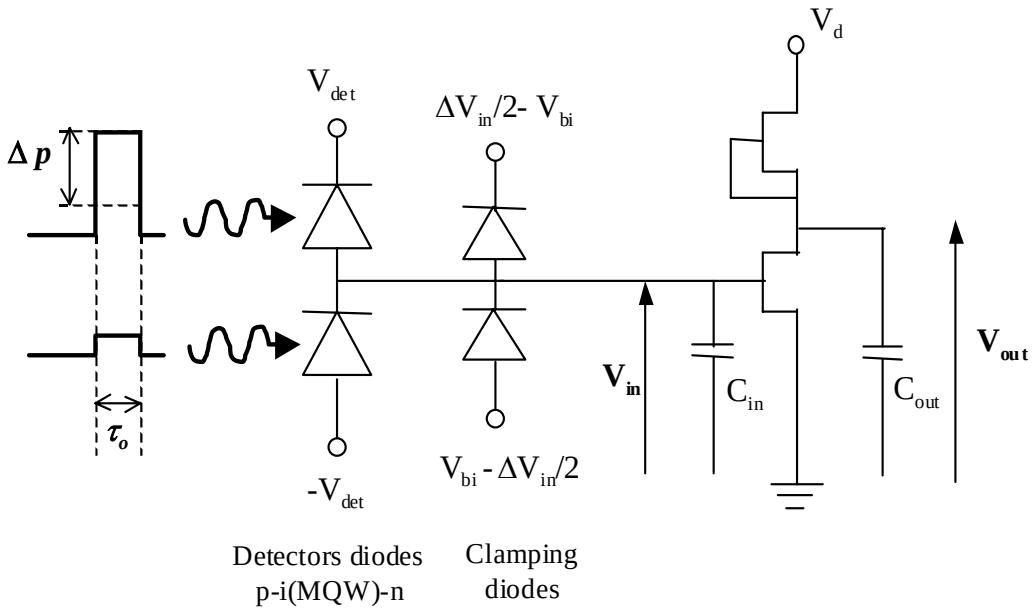

V_d
V_det
ΔV_in/2- V_bi
Δ p
V_in
C_in
C_out
V_out
τ_o
-V_det
V_bi - ΔV_in/2
Detectors diodes
p-i(MQW)-n
Clamping
diodes

FIGURE 9

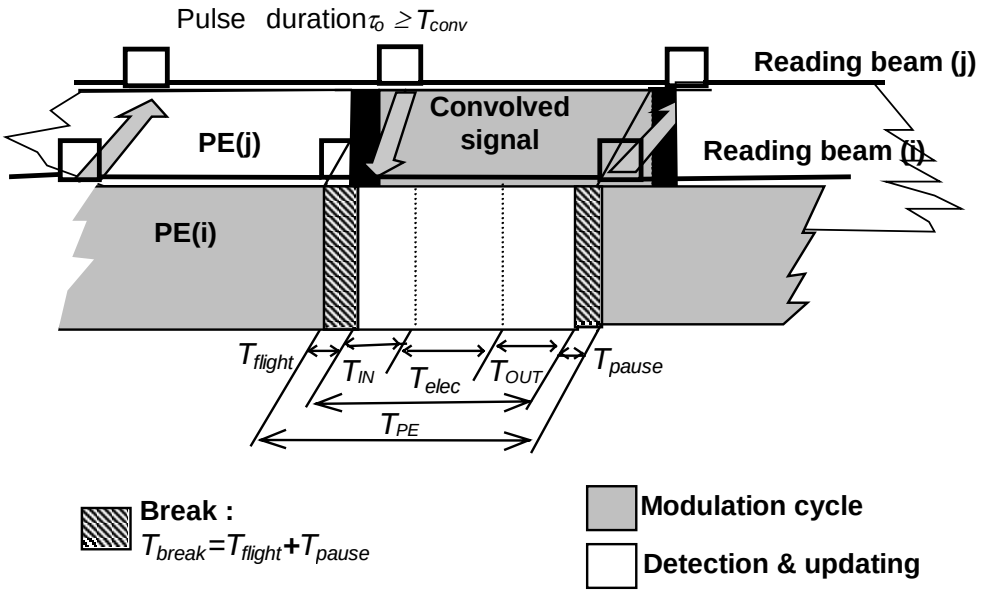

Pulse duration $\tau_0 \geq T_{conv}$
Reading beam (j)
Convolved signal
PE(j)
Reading beam (i)
PE(i)
T_{flight}
T_{IN}
T_{elec}
T_{OUT}
T_{pause}
T_{PE}
Break :
$T_{break}=T_{flight}+T_{pause}$
Modulation cycle
Detection & updating

FIGURE 10

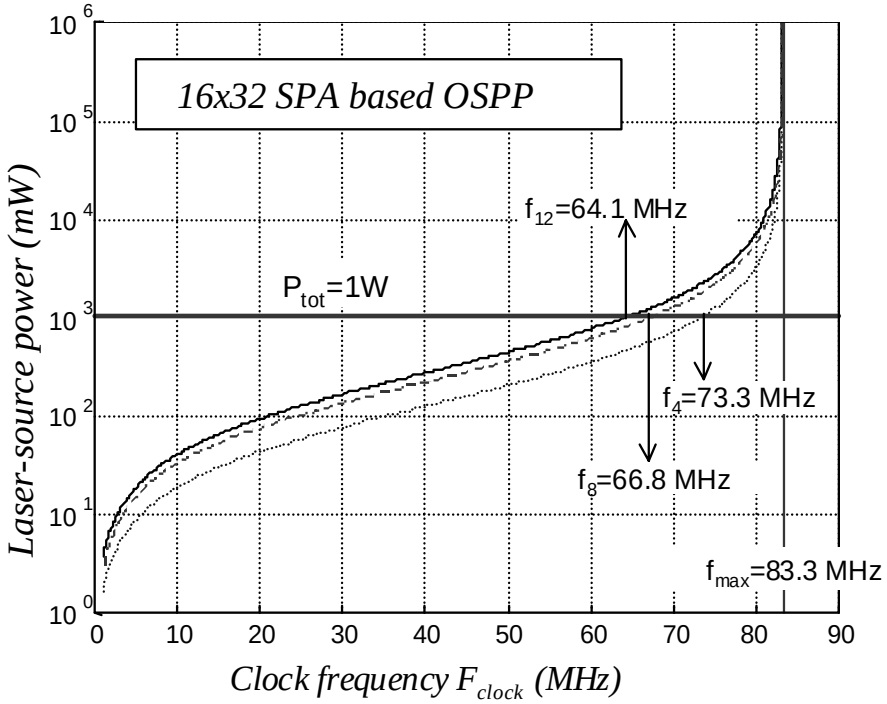

16x32 SPA based OSPP
f_{12}=64.1 MHz
P_{tot}=1W
f_4=73.3 MHz
f_8=66.8 MHz
f_{max}=83.3 MHz
Laser-source power (mW)
Clock frequency F_{clock} (MHz)
10^0
10^1
10^2
10^3
10^4
10^5
10^6
0
10
20
30
40
50
60
70
80
90

FIGURE 11

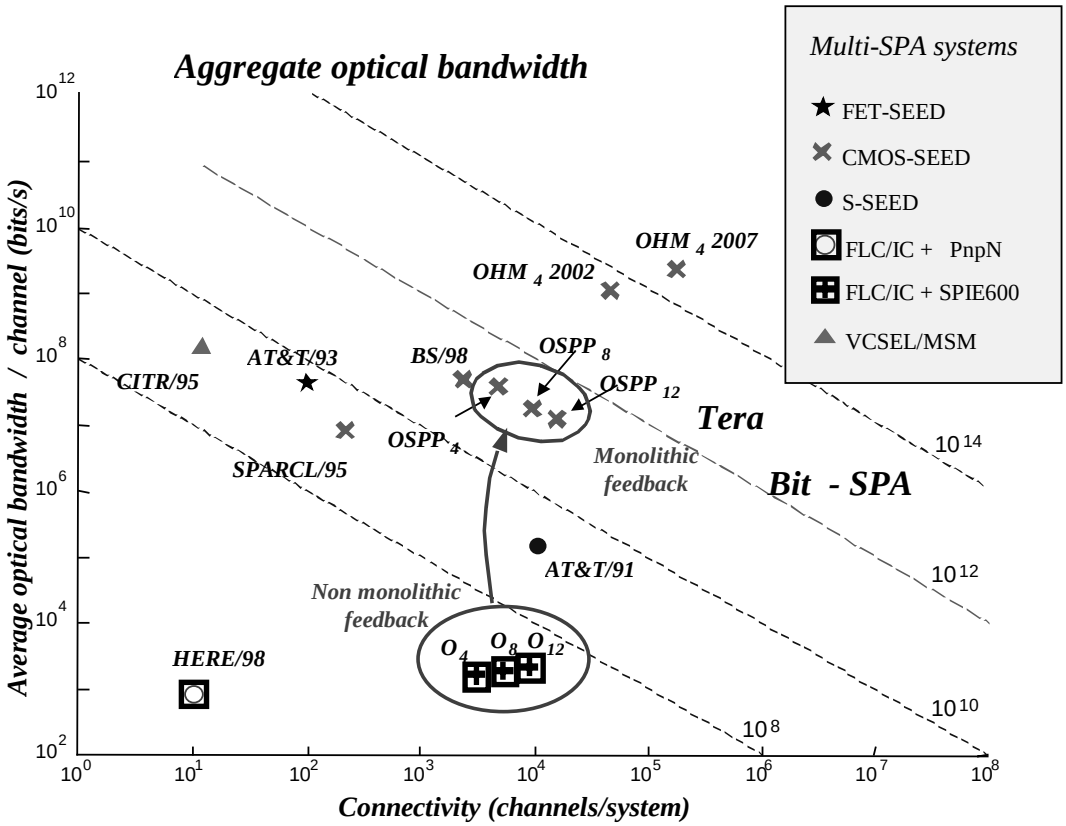

Aggregate optical bandwidth
Multi-SPA systems
FET-SEED
CMOS-SEED
S-SEED
FLC/IC + PnpN
FLC/IC + SPIE600
VCSEL/MSM
Average optical bandwidth / channel (bits/s)
Connectivity (channels/system)
OHM 4 2007
OHM 4 2002
AT&T/93
BS/98
OSPP 8
OSPP 12
CITR/95
OSPP 4
SPARCL/95
Tera
Bit - SPA
Monolithic feedback
AT&T/91
Non monolithic feedback
O4 O8 O12
HERE/98
10 14
10 12
10 10
10 8

FIGURE 12

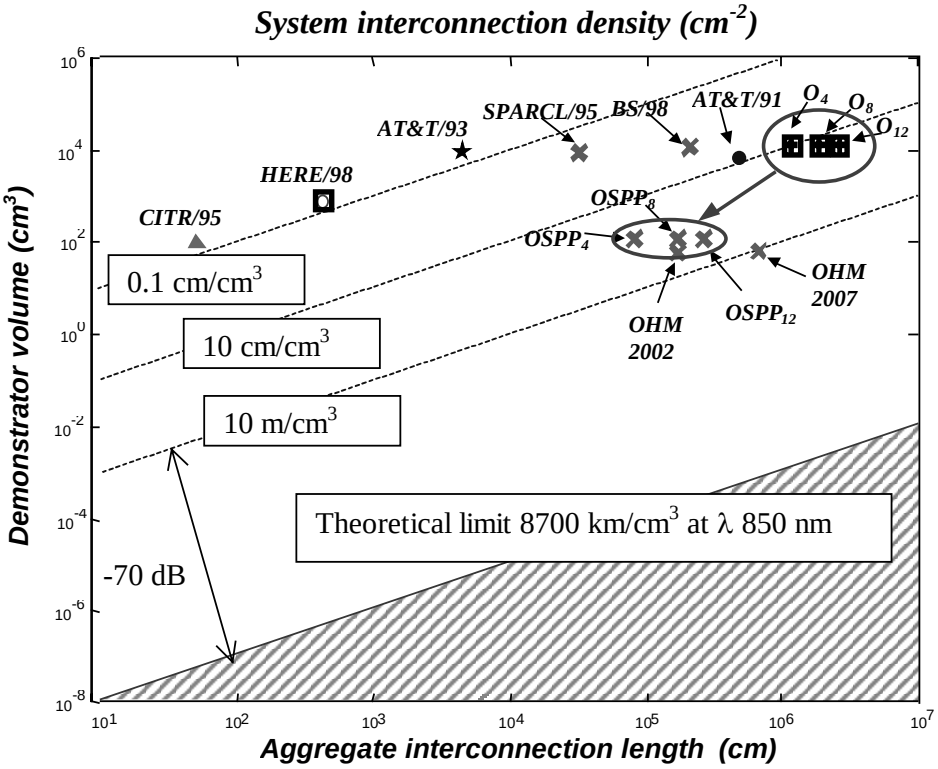

System interconnection density (cm-2)
Demonstrator volume (cm3)
Aggregate interconnection length (cm)
AT&T/93
SPARCL/95
BS/98
AT&T/91
O4
O8
O12
HERE/98
CITR/95
OSPP8
OSPP4
OSPP12
OHM 2007
OHM 2002
0.1 cm/cm3
10 cm/cm3
10 m/cm3
Theoretical limit 8700 km/cm3 at λ 850 nm
-70 dB

FIGURE 13

FIGURE CAPTIONS

Figure 1: PE coloring in the case of a 4 or 8 nearest neighbors interconnection pattern. Interlaced color domains must evolve consecutively, but all pixels in one color domain can evolve in parallel; hence parallelism scales inversely with the number of colors (respectively two and four in the example).

Figure 2: Underlying principles of the simplified motion detection algorithm. The shaded disk represents two consecutive locations of a moving object. Motion information is exclusively provided to the OSPP trough the "observed" binary field $\hat{\boldsymbol{\delta}}(t)$.

Figure 3: Test of the simplified motion-detection algorithm implemented on the (non-monolithic) optically interconnected OSPP prototype. A Dammann grating is in charge of a 8 nearest neighbors optical interconnection pattern. This first prototype relies on a low-resolution, 24x24-pixel large silicon CMOS chip (SPIE600). Gray levels, on a scale of 0 through 255: background=180 / object=220, Gaussian noise: σ=10. Object speed: (1,±2) pixel/frame. Size: Image: 24x24 / moving object: 6x5

Figure 4: Schematic overview of the non-monolithic OSPP demonstrator including an optical input arm (folded), an optical convolution setup (unfolded arm), and an optical random number generator (only the exit of the speckle fiber is represented). Polarizing beam splitters are used to increase the overall system throughput.

Figure 5: A view of the complete setup using the SPIE600 chip. It includes a CCD camera for alignment purposes and continuous monitoring of system operation. Approximate dimensions are 35x21x14 cm^3 (the random number generator hardware is not shown in the picture).

Figure 6: Block diagram of a single OSPP smart-pixel ($\boldsymbol{a_1}$, $\boldsymbol{a_2}$, $\boldsymbol{a_3}$, e and b are one bit memory registers, loaded in parallel over the rows).

Figure7: Optical architecture of the monolithic OSPP. An array illuminator is used to generate a reading bunch of beams to be projected onto the PE modulators. The laser source operates in a q-CW mode. PBSC: polarizing beam-splitter cube; CGH: computer generated hologram; AI: array illuminator; SPA : smart pixel array.

Figure 8: Light from the (global) laser source to a particular p-i-n photodetector - let's say of PE(i) - goes first trough the array illuminator (AI), reflects on every neighboring modulator - i.e., modulators of PE(j), with $j \in N(i)$ - and is diffracted by the computer generated hologram (CGH) before getting to destination.

Figure 9: Single-stage diode clamped receiver. Pulse duration τ_o is 3 or 6 ns, for a minimum (detectable) differential optical power Δp_{min} of 52 or 24 μW respectively.

Figure 10: Chronogram of two neighboring PEs in the case of a two-color array, and corresponding processing latency times.

Figure 11: Optical power requirement versus clock frequency. Continuous line represent the 12-nearest neighbor optically interconnected array; dashed line: 8-nearest neighbor optically interconnected array; dotted line: four nearest neighbor optically interconnected array.

Figure 12: Optical bandwidth improvement of the OSPP demonstrator and comparison with other SPA-based prototypes (CITR/95[37], HERE/98[38], SPARCL/95[39], BS/98[40], AT&T/91[41], AT&T/93[42]). OHM2000/2007 represents perspectives for the CMOS/SEED systems, based on foreseeable improvement in SPA hybrid CMOS/SEED technology [43], and using a compact, rugged Optical Hardware Module as described in[44]. We assumed a 5 SPA system with 2xDOE elements interconnecting adjacent arrays (an architecture equivalent to that of the AT&T/93 demonstrator). FLC/IC : integrated circuit ferroelectric-liquid-crystal modulator; MSM : metal-semiconductor-metal detector. S-SEED : symmetric-SEED[41].

Figure 13: Interconnection density improvements for the monolithic OSPP demonstrator.

TABLES

OSPP performance as a function of the SPA technology.

Technology	**Assumed response time**	**Number of simulated annealing cycles per second (N_C=4)**
The photothyristor array that we tested	26 ms	0.01
SPIE600 (*non monolithic* demonstrator: CMOS chip + liquid crystal SLM)	400 µs	0.6
S-SEED(MQW)	50 µs	5
FET/SEED (MQW)	10 ns	25.000
LED(MQW)/MSM	4 ns	62.500
CMOS/SEED (MQW)	1,6 ns	150.000
VCSEL(MQW)/MSM	1,6 ns	150.000

TABLE 1

Hybrid 32x16 OSPP expected performances

Neighborhood	F_{clock} **(**P_{tot}**=1W)**	***CDR*** **(Mbits/s)**	**S.A. / second**
4 ($OSPP_4$)	73,3 MHz	36,7	36700
8 ($OSPP_8$)	66,8 MHz	16,7	16700
12 ($OSPP_{12}$)	64,1 MHz	12,8	12800

TABLE 2

TABLE CAPTIONS

Table 1: Performance in terms of simulated annealing cycles per second using different technological approaches (a single simulated annealing operation represents *one thousand* updating cycles per color domain, $N_C = 4$ is the number of color domains). There is a gap between *electronic* enhanced detectors (hybrid CMOS / SEED or FET / SEED devices) and simple S-SEED (symmetric-SEED[41]) devices. MSM: Metal-Semiconductor-Metal detector; VCSEL: Vertical cavity surface emitting laser. The photothyristor device that we tested was a preliminary test device and is believed to be far from the limit of that technology.

Table 2: Expected performances for the CMOS/SEED, 32x16 pixel large OSPP. (CDR = smart pixel optical channel data rate; S.A.= Simulated Annealing).

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